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Humphrey et al.

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(45) **Date of Patent: Nov. 5, 2002**

(54) **BALL GRID ARRAY PACKAGE WITH SUPPLEMENTAL ELECTRONIC COMPONENT**

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(73) Assignee: **Agilent Technologies, Inc.**, Palo Alto, CA (US)

(*) Notice: Subject to any disclaimer, the term of this patent is extended or adjusted under 35 U.S.C. 154(b) by 563 days.

(21) Appl. No.: **09/087,130**

(22) Filed: **May 29, 1998**

Related U.S. Application Data

(63) Continuation-in-part of application No. 08/960,735, filed on Oct. 30, 1997.

(51) **Int. Cl.**[7] **H01L 23/48**

(52) **U.S. Cl.** **257/738**; 257/772; 257/778; 257/781

(58) **Field of Search** 257/665, 737, 257/738, 772, 778, 780, 781

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Assistant Examiner—Ori Nadav

(57) **ABSTRACT**

A low inductance integrated circuit package such as a ball grid array package in which is provided a electronic device that enhances performance on an integrated circuit mounted in the die attachment region of the package. The electronic device may be either passive or active and may include such devices as sensors, Zener diodes, voltage regulators, chip based devices, etc. Provision of such devices in a ball grid array package creates a cost effective way of improving the performance on an integrated circuit mounted in that package.

14 Claims, 2 Drawing Sheets

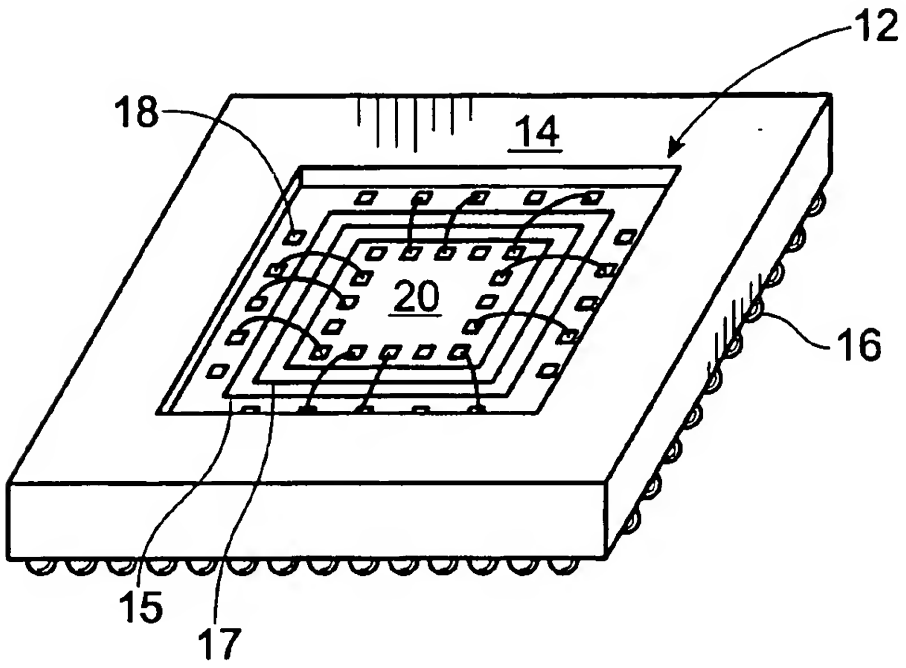


Fig. 1

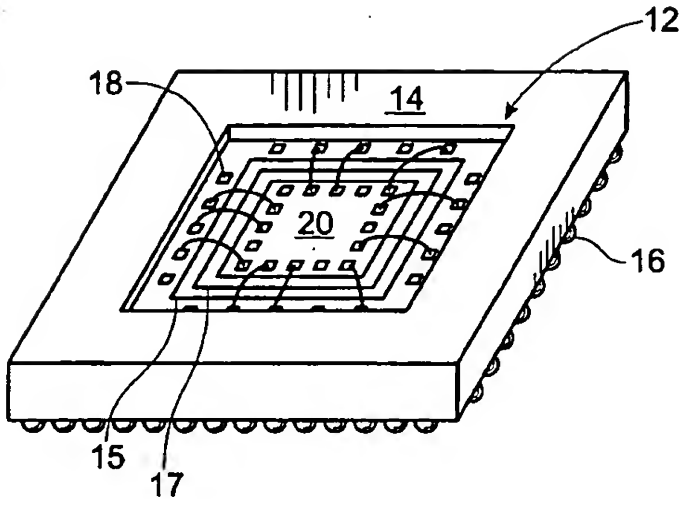


Fig. 2

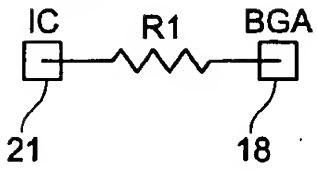


Fig. 3

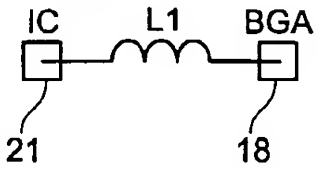


Fig. 4

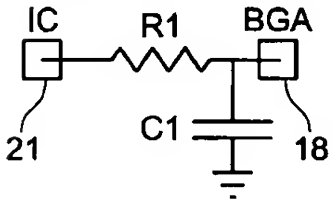


Fig. 5

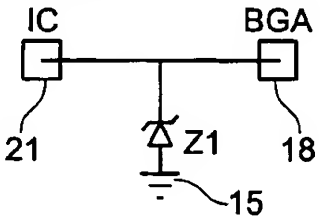


Fig. 6

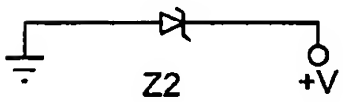


Fig. 7

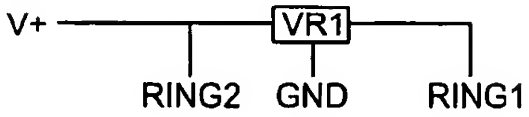
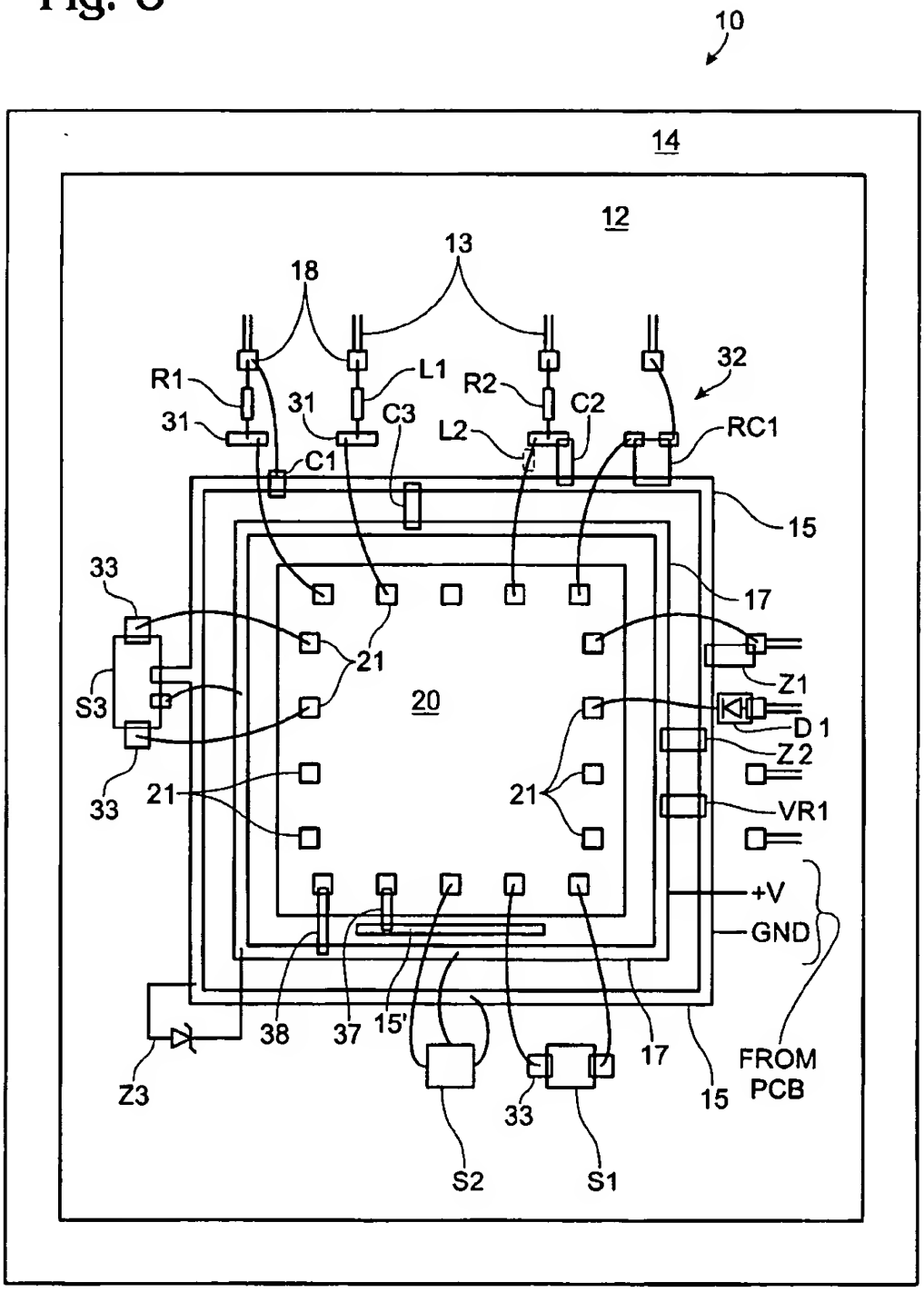


Fig. 8


10
14
12
13
18
32
R1
L1
R2
C2
31
31
C3
L2
RC1
C1
15
33
17
21
Z1
S3
20
D1
Z2
33
21
21
VR1
+V
GND
38
37
15'
17
FROM
PCB
Z3
33
15
S2
S1

BALL GRID ARRAY PACKAGE WITH SUPPLEMENTAL ELECTRONIC COMPONENT

CROSS-REFERENCED TO RELATED APPLICATIONS

The present application is a continuation in part of U.S. patent application Ser. No. 08/960,735, filed Oct. 30, 1997, by Tamio Humphrey and James C. Hudson and entitled Low Noise Ball Grid Array Package.

FIELD OF THE INVENTION

The present invention relates to ball grid arrays and more specifically to enhancing the performance of an integrated circuit mounted in a ball grid array.

BACKGROUND OF THE INVENTION

Ball grid arrays (BGA) and the like are a known type of integrated circuit package. A typical ball grid array includes a platform having a die attachment region provided thereon. The area in which the die attachment region is located is generally referred to as the cavity, while the peripheral area around the cavity is generally referred to as the border. A plurality of contact pads are usually placed towards the periphery of the cavity and these pads are connected by internal conductors to conductive "balls" on the backside (underside when mounted) of the platform. The conductive balls are normally arranged in a grid pattern, hence the name ball grid array, and provide a relatively low inductance electrical connection between the contact pads of the cavity and the traces of a printed circuit board or the like.

Ball grid arrays were developed as a mechanism that (1) facilitates efficient placement, interchangeability and test of integrated circuits and (2) reduces the parasitic lead inductance associated with prior integrated circuit to printed circuit board mountings. Perhaps as a result of this historical development, ball grid arrays are typically viewed merely as a package providing electrical conduits that distribute the pin out of an integrated circuit to appropriate locations on a printed circuit board. Electronic devices that enhance the performance of an integrated circuit, such as filters, regulators, sensors, protection and noise suppression circuits, etc., have conventionally been placed on the printed circuit board to which the integrated circuit and ball grid array are mounted or they are fabricated in the silicon (or other semiconductor material) of the integrated circuit. This practice, however, is disadvantageous in that it uses up valuable printed circuit board and/or integrated circuit real estate. In an effort to alleviate this problem (i.e., to conserve real estate), a designer may choose not to include the componentry, though this results in poorer circuit performance. A need thus exists to utilize ball grid arrays as more than a mere package of distributed conduits in which signal processing is not provided.

SUMMARY OF THE INVENTION

Accordingly, it is an object of the present invention to provide an integrated circuit package such as a ball grid array package that includes one or more supplemental electronic components that enhance the performance of an integrated circuit within the ball grid array package.

It is another object of the present invention to provide an integrated circuit package such as a ball grid array package that has a passive and/or active electronic device provided thereon or therein.

It is another object of the present invention to provide an integrated circuit package such as a ball grid array in which external components are placed close to the integrated circuit, thereby reducing parasitic affects and coupling noise, etc.

It is another object of the present invention to provide an integrated circuit package that affords a low cost, easily implemented manner of providing additional electronic functions inside of the package.

It is also an object of the present invention to provide an integrated circuit package that includes componentry previously placed on a printed circuit board to permit reduction of the size of the printed circuit board and the product in which the printed circuit board is mounted.

These and related objects of the present invention are achieved by use of a ball grid array package with supplemental electronic components as described herein.

In one embodiment, the present invention includes a low inductance integrated circuit package having a platform; a die attachment region formed on a first side of the platform; a plurality of low inductance mounting members form on a second substantially opposite side of the platform; and a supplemental electronic device provided on said first side of the platform that enhances performance on an integrated circuit in said die attachment region.

In another embodiment, the present invention includes a ball grid array apparatus having a platform with a cavity formed on a first side thereof; a die attachment region formed in said cavity; a plurality of low inductance balls formed on a second substantively opposite side of the platform; a ground and a power conductor provided adjacent said die attachment region; and an electronic device coupled to one of said contact pads and provided proximate said die attachment region.

The electronic device may be any passive or active device and may include a resistor, an inductor, a resistor-capacitor circuit, a resistor-capacitor-inductor circuit, an inductor-capacitor circuit, a diode, a Zener diode, and/or a capacitor. In addition the device may be a sensor, a voltage regulator, a chip based device or another electronic device. Provision of the device on a low inductance integrated circuit mounting package provides a cost effective manner of enhancing the performance of an integrated circuit provided in such a package.

A method of forming a low inductance integrated circuit package is also presented.

The attainment of the foregoing and related advantages and features of the invention should be more readily apparent to those skilled in the art, after review of the following more detailed description of the invention taken together with the drawings.

BRIEF DESCRIPTION OF THE DRAWINGS

FIG. 1 is a perspective view of a low inductance integrated circuit mounting package or a ball grid array in accordance with the present invention.

FIGS. 2–7 are schematic diagrams of supplemental electronic componentry that may be provided in the low inductance integrated circuit mounting package or ball grid array of FIG. 1 in accordance with the present invention.

FIG. 8 is a plan view of the low inductance integrated circuit mounting package or ball grid array of FIG. 1 that illustrates supplemental electronic components provided therewith.

DETAILED DESCRIPTION

Referring to FIG. 1, a perspective view of a low inductance integrated circuit mounting package or a ball grid

array **10** in accordance with the present invention is shown. Ball grid arrays are normally made of plastic or ceramic or other suitable material as is known. Ball grid array **10** is preferably made of plastic to facilitate the low cost production of integrated circuit packaging. The use of supplemental electronic components as discussed herein in combination with a low cost package achieves a low cost manner of improving circuit performance.

Ball grid array **10** includes a die attachment region or cavity **12**, which is preferably surrounded by a border **14**. A plurality of conductive balls **16** are provided on a mounting surface of the ball grid array and these balls are connected through internal conductors to exposed contact pads **18** in cavity **12**. An integrated circuit **20** is mounted within cavity **12** using known mounting techniques and a ground ring **15** and a power ring **17** or the like are typically provided around the integrated circuit for delivery of these signals to the circuit. The ground and power rings may be partial, fragmented or complete. A plurality of contact pads **21** (labeled in FIG. **8**) are shown around the periphery of integrated circuit **20**. These pads are preferably connected to contact pads **18** of the ball grid array and to the supplemental electronic components (discussed below) by wire leads. To reduce crowding in FIG. **1**, less than the conventional number of contact pad and wire leads are shown and the leads and contact pads **21** are not labeled.

As discussed in more detail below with reference to FIGS. **2–8**, one or more circuit components are provided on ball grid array **10**, preferably within cavity **12**, to enhance the performance of integrated circuit **20**. It is to be understood that the components of FIGS. **2–8** are implemented in cavity **12** of ball grid array **10** of FIG. **1**.

Referring to FIG. **2**, a schematic diagram of a supplemental resistor **R1** provided in an integrated circuit package such as a ball grid array package in accordance with the present invention is shown. Resistor R1 is preferably any of a type of known resistive elements including chip resistors, conductive strip resistors, etc. Resistor R1 is coupled between a contact pad **18** of the ball grid array and contact pad **21** of the integrated circuit.

Referring to FIG. **3**, a schematic diagram of a **30** supplemental inductor **L1** provided in an integrated circuit package such as a ball grid array package in accordance with the present invention is shown. Inductor L1 is preferably any of a type of known surface mount inductors or the like and is coupled between a ball grid array contact pad **18** and an integrated circuit pad **21**.

Referring to FIG. **4**, a schematic diagram of a supplemental resistor-capacitor circuit provided in an integrated circuit package such as a ball grid array package in accordance with the present invention is shown. The resistor-capacitor circuit may function as a filter circuit and may be comprised of discreet components R1,C1 or provided as a chip RC circuit (RC1 of FIG. **8**), etc.

Referring to FIG. **5**, a schematic diagram of a supplemental signal line coupled Zener diode **Z1** provided in an integrated circuit package such as a ball grid array package in accordance with the present invention is shown. Zener diode **Z1** provides signal line noise suppression or reduction and is preferably coupled to a signal line between contact pads **18,21** in such a manner as to shunt over currents in that signal line to ground. Suitable surface mount Zener diodes or the like or related noise suppression devices are known in the art.

Referring to FIG. **6**, a schematic diagram of a supplemental power conductor Zener diode **Z2** provided in an integrated circuit package such as a ball grid array package in accordance with the present invention is shown. Zener diode Z2 or like components provide noise suppression or reduction in the power conductor and function by shunting overcurrents in the power supply network to ground. Zener diode Z2 is preferably coupled between the power and ground rings **17,15**.

Referring to FIG. **7**, a schematic diagram of a supplemental voltage regulator provided in an integrated circuit package such as a ball grid array package in accordance with the present invention is shown. Voltage regulator VR1 is preferably provided between the power supply conductor(s) and ground. Suitable voltage regulators and the like are known in the art.

Referring to FIG. **8**, a plan view of a low inductance integrated circuit. mounting package or a ball grid array package having supplemental electronic components in accordance with the present invention is shown. Several of the features or elements shown in FIG. **1** are shown in FIG. **8**. These include cavity **12**, border **14**, ground ring **15**, power ring **17**, contact pads **18** and integrated circuit **20**.

A plurality of conductive traces **13** are shown coupled to contact pads **18**. These are exposed portions of the internal conductors that connect conductive balls **16** (FIG. **1**) to contact pads **18**. Ball grid array **10** may also contain internal conductors that are wholly unexposed (connecting through vias to the underside of a contact pad **18**).

As alluded to above, the present invention includes providing components on or within ball grid array **10** that enhance circuit performance. The components may perform functions related to filtering, noise suppression, signal generation or other. While the components may be added within the ball grid array during fabrication, in a preferred embodiment the components are mounted in or near the exposed cavity region after initial BGA formation. Such a practice provides many benefits including, but not limited to, formation of non-custom ball grid array packages, reduced ball grid array fabrication costs, ease of access to components and their placement locations and interchangeability of components, etc. The components may be active and/or passive as discussed in more detail below and may be provided as discreet devices or within integrated circuits or "chips". The components are preferably surface mounted using standard surface mount assembly techniques. Several representative components and representative arrangements are now discussed. The representative examples are intended to be illustrative of various embodiments of the present invention and to be in no way limiting. It would be evident to one skilled in the art to utilize other types of components in or on a ball grid array to achieve a desired signal processing given the teachings herein.

Referring more specifically to the upper left hand corner of FIG. **8**, an implementation of R1 (of FIG. **2** or FIG. **4**) is shown. **R1** is coupled between a contact pad **18** and a supplemental contact pad **31**. The supplemental contact pad is coupled to a contact pad **21** of the integrated circuit. Supplemental contact pads (**31,32,33**) are essentially conductive areas formed on an exposed surface of the ball grid array and may be provided in a uniform or non-uniform pattern. The supplemental contact pads provide additional surfaces for mounting some of the supplemental electronic components discussed herein.

Capacitor **C1** is shown coupled to (i.e., mounted on) ground ring **15** and the same contact pad **18** to which **R1** is connected. The arrangement of C1 is this manner forms the resistor-capacitor circuit of FIG. **4**.

Inductor L1 is shown coupled between a contact pad **18** and a supplemental contact pad **31** that is in turn coupled to a contact pad of the integrated circuit. A capacitor C3 is shown coupled between the ground and power rings **15,17** for EMI suppression.

Components R2,L2,C2 form a RLC filter circuit. The inductor may be a surface mount device or the like or an inherent characteristic of the wire lead that connects between the supplemental contact pad and the integrated circuit. Capacitor C2 is shown coupled between the supplemental contact pad and the ground ring as opposed to being mounted on the ground ring like C1.

RC1 represents a chip RC circuit. If desired the chip of RC1 could be fabricated to include an inductor or another arrangement of devices. A paired supplemental contact pad **32** is provided to signal line input and output. Chip RC1 is also coupled to the ground ring.

Zener diode Z1 is coupled between a contact pad **18** of the ball grid array and a contact pad **21** of the integrated circuit. Z1 provides signal line noise suppression.

Zener diode Z2 is provided between the ground and power conductors **15,17** and provides a similar function. A voltage regulator VR1 may also be provided between the ground and power conductors.

S1, S2 and S3 represent sensors. Sensor S1 is coupled to random supplemental contact pads **31** and between first and second signal lines (e.g., input and output) of integrated circuit **20**. Sensor S2 receives power and ground and outputs a signal to the integrated circuit. Sensor S3 is coupled between a first and a second signal and receives power and ground.

Sensors S1–S3 may be temperature, light, current or voltage or other types of sensors or the like and may function as stand alone units or in combination with other known circuit components, not shown. The sensors preferably provide information related to integrated circuit performance. For example, sensor **56** may be a temperature sensor and logic within integrated circuit **20** may be programmed to operate at a reduced power mode when sensor **56** indicates a temperature that is above a predetermined threshold.

Sensors S1–S3 are presented as examples of the present invention. It should be recognized that the components indicated as S1–S3 could alternatively be another electronic, electromechanical or electromagnetic device including an integrated circuit performing a non-sensing function, etc. Placement of various components including smaller surface mount integrated circuits and/or other devices within a ball grid array package permits the formation of low cost packages with enhanced circuit performance.

In normal use, integrated circuit **20** typically has many more contact pads **21** than those shown. These contact pads are connected by wire lead lines to contact pads **18** of the ball grid array and to the ground and power conductors as appropriate. Due to the presence of these wire lead lines, the arrangement or placement of the various supplemental components discussed herein must accommodate requisite lead line connections. Hence, the provision of supplemental components near the corners or other regions of the cavity in which they do not interfere with connecting lead lines is preferred. Zener diode Z3 is shown in the lower left-hand corner.

FIG. **8** also illustrates a supplemental ground conductor **15'** and an electronic device **37** coupled between that conductor and a contact pad **21**. An electronic device **38** is also shown between power conductor **15** and a contact pad **21**. Electronic devices **37,38** may be pull up or pull down resistors or capacitors or any other suitable electronic device. A representative diode D1 is also illustrated in FIG. **8**. The diode may be coupled within a signal line or otherwise as known in the art.

While the invention has been described in connection with specific embodiments thereof, it will be understood that it is capable of further modification, and this application is intended to cover any variations, uses, or adaptations of the invention following, in general, the principles of the invention and including such departures from the present disclosure as come within known or customary practice in the art to which the invention pertains and as may be applied to the essential features hereinbefore set forth, and as fall within the scope of the invention and the limits of the appended claims.

What is claimed is:

1. A low inductance integrated circuit package, comprising:

a platform having a first side and a second side, said second side being disposed generally opposite said first side;

a cavity region formed on said first side of said platform, said cavity being substantially surrounded by a border region and including a die attachment region positioned therein;

a plurality of contact pads provided at said cavity region for coupling to an integrated circuit provided at said die attachment region;

a plurality of low inductance mounting members for electrically mounting said platform, each of said low inductance mounting members being coupled to one of said plurality of contact pads via internal conductors;

a power conductor provided at said cavity region proximate said die attachment region and coupled to at least one of said low inductance mounting members, said power conductor being provided on substantially all horizontally disposed sides of said die attachment region;

a ground conductor provided at said cavity region proximate said die attachment region and coupled to at least one of said low inductance mounting members, said ground conductor being provided on substantially all horizontally disposed sides of said die attachment region; and

a supplemental electronic device provided at said cavity region at least in part between said die attachment region and said border region that enhances performance on an integrated circuit in said die attachment region, said supplemental electronic device includes one or more of the group of electronic devices including:

a resistor;

an inductor;

a resistor-capacitor circuit;

a resistor-capacitor-inductor circuit;

an inductor-capacitor circuit;

a sensor;

a diode;

a Zener diode; and

an active device.

2. The integrated circuit mounting package of claim **1**, wherein said power and ground conductors are provided in a substantially parallel relationship with one another at said cavity region.

3. The integrated circuit mounting package of claim **1**, further comprising an integrated circuit mounted at said die

attachment region and wherein said supplemental electronic device is a sensor that functions in conjunction with said mounted integrated circuit.

4. The integrated circuit mounting package of claim 1, wherein said supplemental electronic device is provided in an integrated circuit.

5. The integrated circuit mounting package of claim 1, wherein said supplemental electronic device is coupled at said cavity region to at least one of said power and ground conductors.

6. The integrated circuit mounting package of claim 1, wherein said low inductance mounting members are provided on said second side of said platform.

7. The integrated circuit mounting package of claim 1, wherein said cavity is recessed.

8. A low inductance integrated circuit package apparatus, comprising:

a platform having a first side and a second side, said second side being disposed generally opposite said first side;

a die attachment region formed on said first side of said platform;

a plurality of contact pads provided about said die attachment region for coupling to an integrated circuit provided at said die attachment region;

a plurality of low inductance mounting members formed on said platform, each coupled by an internal conductor to one of said plurality of contact pads;

a power conductor provided on said first side of said platform and on substantially all horizontally disposed sides of said die attachment region;

a ground conductor provided on said first side of said platform and on substantially all horizontally disposed sides of said die attachment region; and

an electronic device coupled to one of said contact pads and provided adjacent said die attachment region, said electronic device provided to enhance performance on an integrated circuit mounted at said die attachment region, said electronic device includes including or more of the group of electronic devices including:

a resistor;

an inductor;

a resistor-capacitor circuit;

a resistor-capacitor-inductor circuit;

an inductor-capacitor circuit;

a sensor;

a diode;

a Zener diode; and

an active device.

9. The apparatus of claim 8, wherein said die attachment region is surrounded by a border region formed towards the periphery of the platform and said electronic device is provided proximate said die attachment region substantially between said die attachment region and said border region.

10. The apparatus of claim 8, wherein said electronic device is a sensor that functions in conjunction with an integrated circuit provided in said die attachment region.

11. The apparatus of claim 1, wherein said electronic device is provided in an integrated circuit.

12. The apparatus of claim 1, wherein said low inductance mounting members are provided on said second side of said platform.

13. The apparatus of claim 8, wherein said electronic device is coupled to at least one of said power and ground conductors.

14. The apparatus of claim 8, wherein said power and ground conductors are arranged in a substantially parallel manner about said die attachment region.

* * * * *

US006175509B1

(12) **United States Patent**
Koch

(10) **Patent No.: US 6,175,509 B1**
(45) **Date of Patent: *Jan. 16, 2001**

(54) **SPACE EFFICIENT LOCAL REGULATOR FOR A MICROPROCESSOR**

(75) Inventor: **James K. Koch**, Rocklin, CA (US)

(73) Assignee: **Hewlett-Packard Company**, Palo Alto, CA (US)

(*) Notice: This patent issued on a continued prosecution application filed under 37 CFR 1.53(d), and is subject to the twenty year patent term provisions of 35 U.S.C. 154(a)(2).

Under 35 U.S.C. 154(b), the term of this patent shall be extended for 0 days.

This patent is subject to a terminal disclaimer.

(21) Appl. No.: **08/856,312**

(22) Filed: **May 14, 1997**

(51) **Int. Cl.**[7] **H05K 7/02**; H05K 1/16; H01R 4/60

(52) **U.S. Cl.** ..... **361/809**; 174/260; 174/71 B; 174/72 B; 361/807; 361/810; 361/775; 439/212

(58) **Field of Search** ..... 174/260, 71 B, 174/72 B, 88 B, 99 B, 70 B; 361/748, 760, 761, 762, 807, 809, 811, 753, 772, 773, 774, 783, 789, 803, 826, 775; 439/212

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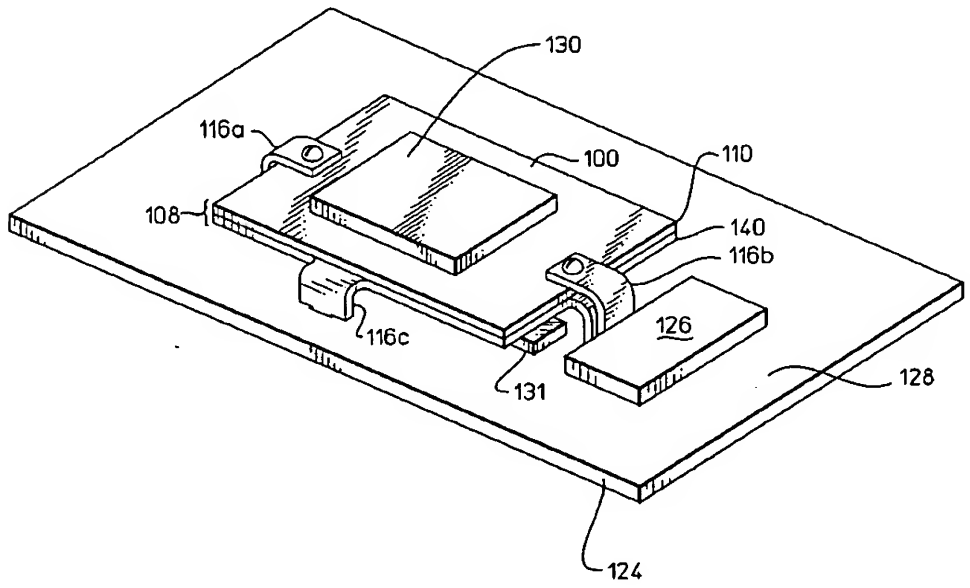
Primary Examiner—Hyung-Sub Sough
(74) *Attorney, Agent, or Firm*—Denise A. Lee

(57) **ABSTRACT**

The present invention is a mounting platform for placement of a first device on a first plane in close proximity to a second device on a second plane. In the preferred embodiment, the first device is a voltage regulator circuit, the second device is a microprocessor, the first plane is the surface of the platform printed circuit board (PCB), and the second plane is the surface of the base printed circuit board. Typically the microprocessor is electrically coupled to the base printed circuit board and the voltage regulator circuit is electrically coupled to the platform printed circuit board. The mounting platform is mounted as a mezzanine over the base printed circuit board on the platform printed circuit board. Mounting the voltage regulator in this way allows the voltage regulator output to be placed adjacent to the microprocessor chip while at the same time minimizing the amount of valuable board space that is used.

15 Claims, 5 Drawing Sheets



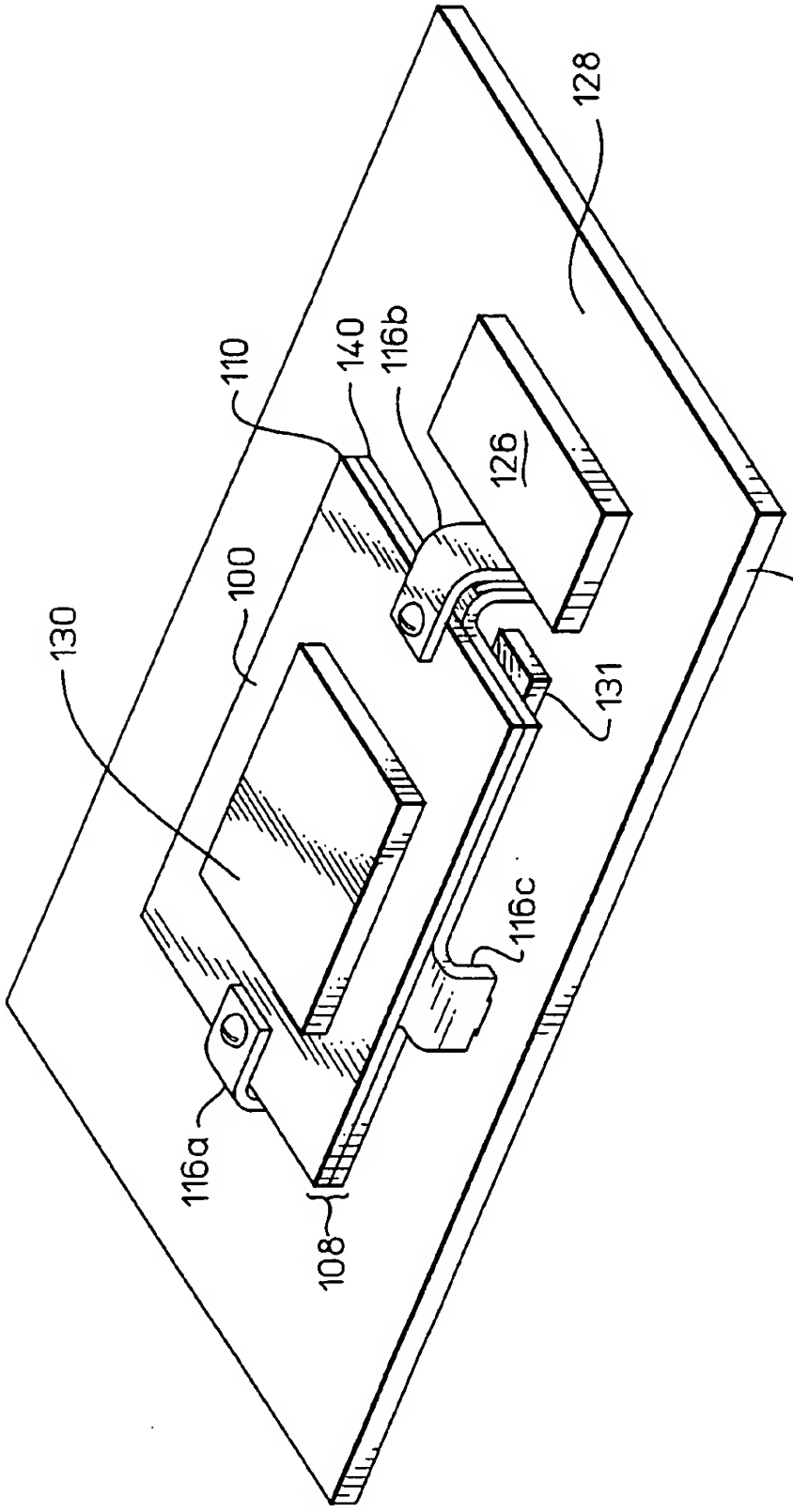


Figure 1

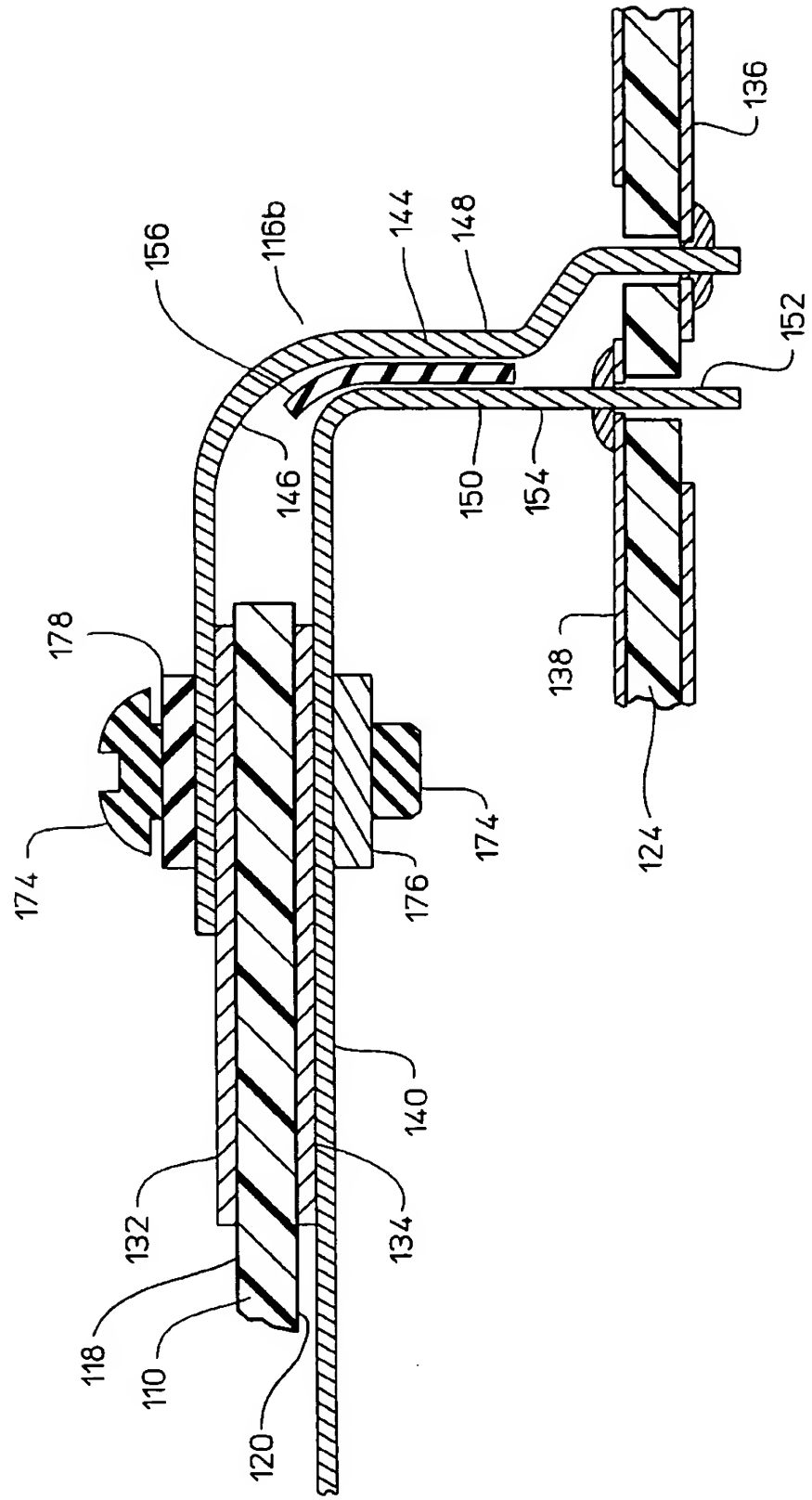

136
156
116b
144
148
152
146
150
154
138
178
174
174
176
124
140
132
134
118
110
120

Figure 2

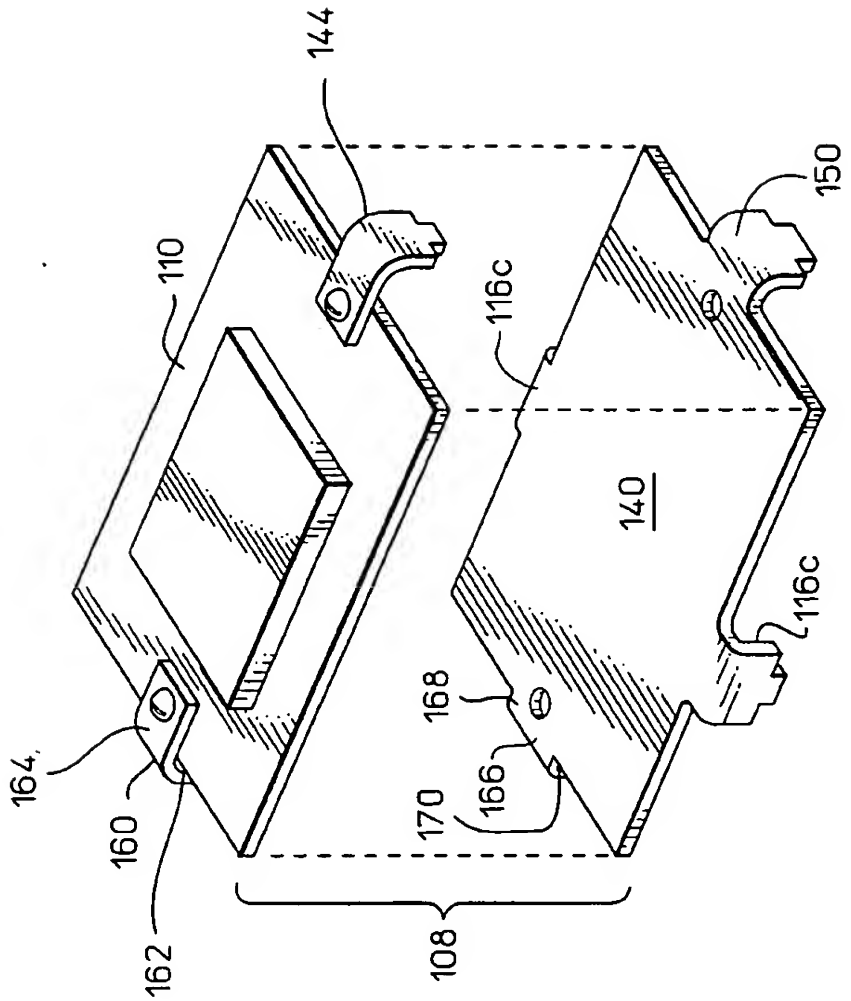


Figure 3

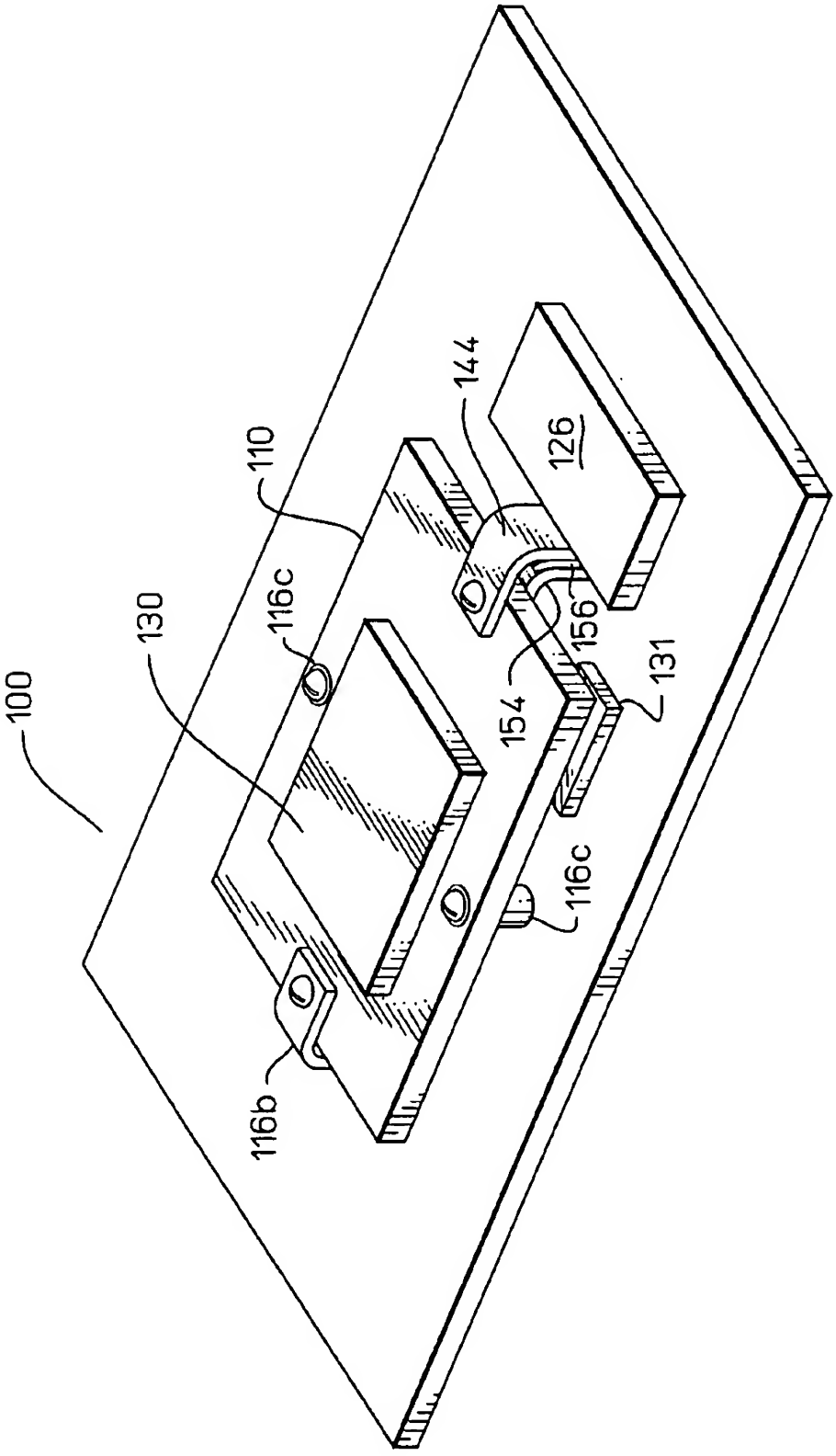


Figure 4

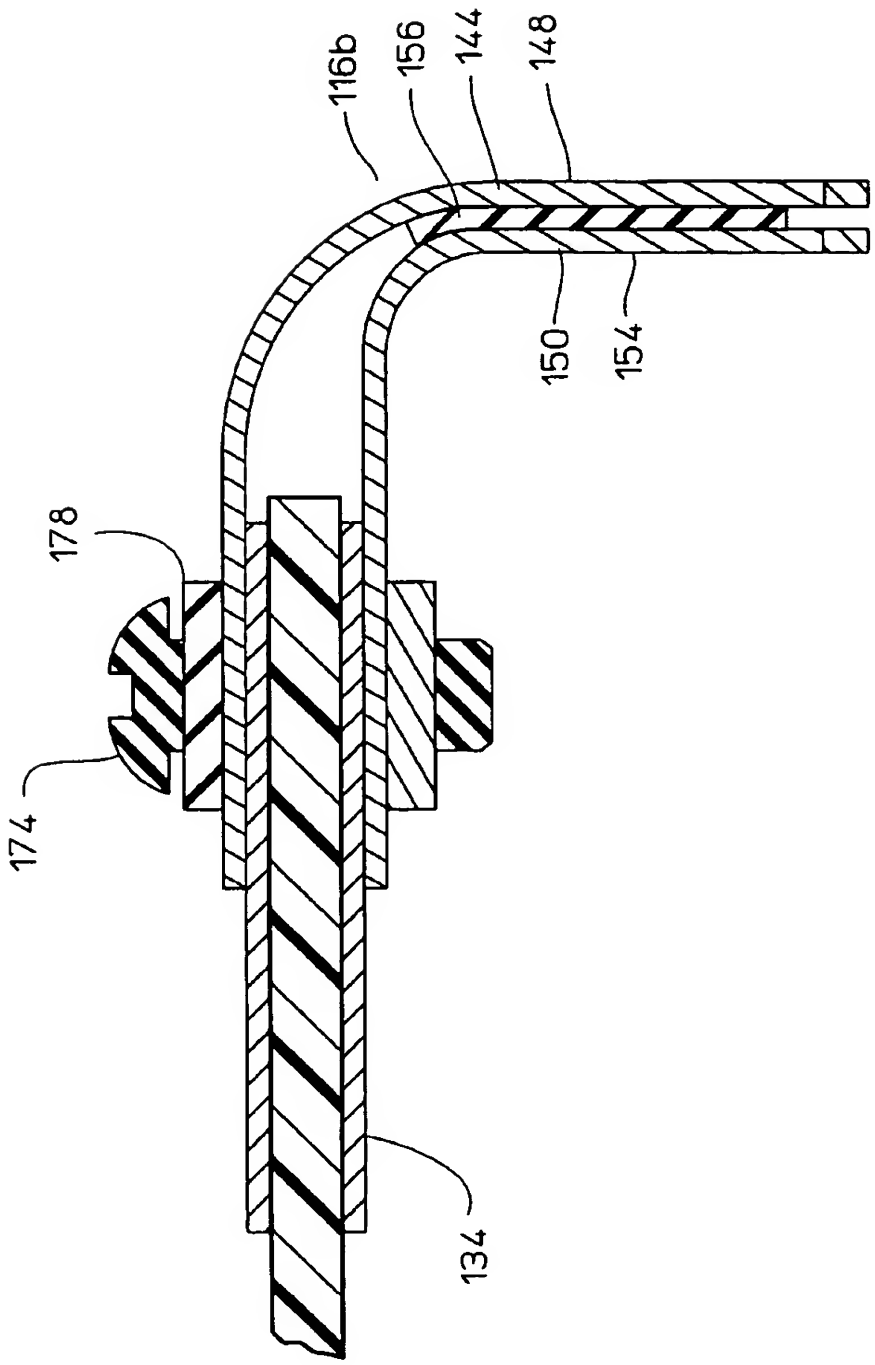


Figure 5

SPACE EFFICIENT LOCAL REGULATOR FOR A MICROPROCESSOR

REFERENCE TO RELATED APPLICATION

Reference is made to the following co-pending and commonly assigned U.S. patent application entitled: POWER BUS BAR FOR PROVIDING A LOW IMPEDANCE CONNECTION BETWEEN A FIRST AND SECOND PRINTED CIRCUIT BOARD, Ser. No. 08/856,500, now U.S. Pat. No. 6,024,589 May 14, 1997.

BACKGROUND OF THE INVENTION

Modern microprocessors require the output of high current at relatively low voltage levels, typically in the range of zero to five volts. Further, although microprocessor requires high current, the current demands for requirements fluctuate widely. For example, in the sleep or idle mode a microprocessor might require currents in the range of 0.5 A to 5 A while a microprocessor in a faster computing mode might require currents in the range of 10 A to 100 A. However even though current requirements fluctuate widely, microprocessor specifications require that the voltage limits remain relatively stable, no matter what the operational mode of the microprocessor.

Requirements for tight voltage regulation in response to highly variable current demands mean that the main power supply output can no longer be fed directly to the microprocessor. Instead, a voltage regulator is used to deliver a tightly controlled voltage to the microprocessor. A local voltage regulator supplies a high level of DC current and minimizes the uncertainty in voltage drops between the main power supply and the microprocessor.

Although a voltage regulator circuit provides tight voltage regulation, it must be placed in close proximity to the microprocessor. If the voltage regulator is too far from the microprocessor, impedance between the voltage regulator and microprocessor increases, causing poor voltage regulation at the microprocessor. Further, an increase in impedance decreases speed and increases voltage drops. As the clock speed requirements for microprocessors increase, increases in impedance become less and less acceptable.

A problem with positioning the voltage regulator circuit in close proximity to the microprocessor is that other peripheral devices that work with the microprocessor may be displaced. For example, memory chips, etc. also need to be in close proximity to microprocessor. Thus, the voltage regulator circuit uses up a significant amount of board space which could otherwise be used effectively for the placement of cache memory or other integrated circuits peripheral to the microprocessor, which also need to be close to the microprocessor for reasons of signal integrity. Further, because space constraints are so tight, it is difficult to customize a board for the customer by adding different optional components since board space near the microprocessor is so limited.

A method and apparatus for locating a voltage regulator circuit close to microprocessor while minimizing the required board space and minimizing impedance is needed.

SUMMARY OF THE INVENTION

The present invention is a mounting platform for placement of a first device on a first plane in close proximity to a second device on a second plane. In the preferred embodiment, the first device is a voltage regulator circuit, the second device is a microprocessor, the first plane is the surface of the platform printed circuit board (PCB), and the second plane is the surface of the base printed circuit board. Typically the microprocessor is electrically coupled to the base printed circuit board and the voltage regulator circuit is electrically coupled to the platform printed circuit board. The mounting platform is mounted as a mezzanine over the base printed circuit board on the platform printed circuit board. Mounting the voltage regulator allows the voltage regulator output to be placed adjacent to the microprocessor chip while at the same time minimizing the amount of valuable board space that is used.

The mounting platform forms a "table" over the second plane and is typically comprised of a platform top and a plurality of elongate legs that are soldered or otherwise connected to the platform top. Typically, the platform top of the mounting platform includes of a platform printed circuit board having a power plane and a ground plane. Similarly, the base printed circuit board also includes a power plane and a ground plane. The plurality of elongate legs electrically connect the power plane of the platform PCB to the power plane of the base PCB and electrically connect the ground plane of the platform PCB to the ground plane of the base PCB.

The plurality of elongate legs that are connected to the platform top typically includes an output power leg, an input power leg, and at least a first support leg. Both the input power leg and the output power leg are comprised of a first conductor, a second conductor and an insulator positioned between the first and second conductors. The first and second conductors of the input and output power legs form a low impedance transmission line. The high dielectric constant of the insulator positioned between the first and second conductors provides distributed capacitance between the first and second conductors, lowering the AC impedance and improving the transient response.

Preferably, the first input conductor and the first output conductor are electrically coupled to the power plane of the platform printed circuit board. Similarly, the second input conductor and the second output conductor are electrically coupled to the ground plane of the platform printed circuit board. The input power leg of the mounting platform carries power to the voltage regulator. The output power leg of the mounting platform carries the output power of the voltage regulator to the microprocessor.

In the preferred embodiment, the platform top is comprised of a platform printed circuit board and a platform conductive frame. In the preferred embodiment, the second input conductor and the second output conductors extend from a unitary platform conductive frame that is electrically connected to the ground plane of the platform printed circuit board. The second output conductor and the second input conductors extend from and form part of the unitary platform conductive frame structure. Typically, the platform conductive frame is positioned underneath the platform printed circuit board. Preferably, the platform conductive frame is used as a ground plane for the voltage regulator circuit and for conducting ground current to the microprocessor through one or more of the "legs" of the mounting platform. Because the platform conductive frame acts as ground, the ground plane of the platform printed circuit board is no longer required.

The mounting platform offers a practical and cost-efficient way to locate a very high current voltage regulator in close proximity to the microprocessor chip without significantly reducing the amount of board space available for logic circuits peripheral to the microprocessor. The mounting

platform is mechanically stable and is resistant to high levels of shock and vibration. Further, the conductive portions of the legs and the platform conductive frame of the mounting platform act as heat sinks, providing increased cooling for the system. In addition, the platform conductive frame and the platform legs of the mounting platform provide shielding to isolate the voltage regulator circuit from the microprocessor circuit.

A further understanding of the nature and advantages of the invention described herein may be realized by reference to the remaining portions of the specification and the drawings.

BRIEF DESCRIPTION OF THE DRAWINGS

FIG. **1** shows the mounting platform according to the preferred embodiment of the present invention.

FIG. **2** shows a side cross-sectional view of the output leg of the mounting platform shown in FIG. **1**.

FIG. **3** shows a partial exploded view of the mounting platform shown in FIG. **1**.

FIG. **4** shows a mounting platform according to an alternative embodiment of the present invention.

FIG. **5** shows a side cross-sectional view of the output leg of the mounting platform shown in FIG. **4**.

DETAILED DESCRIPTION OF THE PREFERRED EMBODIMENTS

FIG. **1** shows a mounting platform **100** according to a first embodiment of the invention. The mounting platform **100** is comprised of a platform top **108** including a platform printed circuit board **110** that includes a first electrical contact **132** and a second electrical contact **134** and a plurality of elongate legs including an input leg **116***a*, an output power leg **116***b*, and at least a first support leg **16***c*. The platform printed circuit board **110** has a first surface **118** and a second surface **120**. Typically, the first electrical contact **132** is formed on the first surface **118** of the platform printed circuit board **110** and the second electrical contact **134** is formed on the second surface **120** of the platform printed circuit board **110**.

In the preferred embodiment the mounting platform **100** is mechanically and electrically coupled to a base printed circuit board **124**. The mounting platform **100** is configured so that a second device **126** on the first surface **128** of the base PCB **124** is in close proximity to a first device **130** on the first surface of the **118** of the platform PCB **110**. In the preferred embodiment, the first device **130** is a voltage regulator circuit, the second device **126** is a microprocessor, the first plane is the first surface **118** of the platform printed circuit board (PCB), and the second plane is the first surface **128** of the base printed circuit board. The voltage regulator **130** is mounted on a first surface **118** of the platform printed circuit board **110** and is electrically coupled to the platform printed circuit board **110** while the microprocessor **126** is mounted to and electrically coupled to the first surface **128** of the base printed circuit board **124**.

Mounting the voltage regulator circuit **130** over the base printed circuit board **124** allows both the voltage regulator **130** and other peripheral logic chips **131** to be positioned close to the microprocessor **126**. The mounting platform can be placed close to the load without using a significant amount of board space near the load. This is advantageous in circuits such as microprocessors which are high speed and which use relatively large currents at a low voltage.

Theoretically, the entire mounting platform or a portion of the mounting platform could be physically located over the microprocessor. However, for reasons including efficient heat dissipation, etc. the mounting platform is not placed directly over the microprocessor. Instead, the mounting platform **100** is typically placed adjacent to the microprocessor **126**. The output power leg **116***b* of the mounting platform, the leg carrying power from the voltage regulator to the microprocessor, should be placed as close to the microprocessor **126** as possible.

FIG. **2** shows a side cross-sectional view of the output leg **116***b* of the mounting platform shown in FIG. **1**. Referring to FIG. **2** shows that the platform printed circuit board **110** includes a first electrical contact **132** and a second electrical contact **134**. The first electrical contact **132** is formed on the first surface of the platform PCB **110** and is typically connected to the platform power plane. Power plane means an electrical network which connects a common voltage to a number of circuit nodes. The platform PCB and the base PCB may have a plurality of power planes and may have a corresponding electrical contact for each of the power plane.

The second electrical contact **134** is formed on the second surface of the platform PCB **110** and is typically connected to the platform ground plane. Similarly, the base PCB typically includes a first electrical contact **136** and a second electrical contact **138**. The first electrical contact **136** is formed on the second surface of the base PCB **124** and is typically connected to the base power plane while the second electrical contact **138** is formed on the first surface **128** of the base PCB and is typically electrically connected to base ground plane.

The mounting platform **100** includes a plurality of elongate legs **116***a*–**116***c*, including at least an output power leg **116***b*. Preferably, the mounting platform **100** further includes an input power leg **116***a* and a support leg **116***c*. The output power leg **116***b* includes a first output conductor having a first surface **146** and a second surface **148**, a second output conductor **150** having a first surface **152** and a second surface **154**, and an output power insulator **156** positioned between the first surface **146** of the first output conductor **144** and the first surface **152** of the second output conductor **150**. Similarly, the input power leg **116***a* includes a first input conductor **160** having a first surface **162** and a second surface **164**, a second input conductor **166** having a first surface **168** and a second surface **170**, and an input power insulator (not shown) positioned between the first surface **162** of the first input conductor **160** and the first surface **168** of the second input conductor **166**. Typically the input and output conductors are made of solid, copper with plating suitable for electrical contact.

The first and second output conductors **144**, **150** and the first and second input conductors **160**, **166** form low impedance transmission lines at high frequencies. Thus, preferably the output power insulator **156** and the input power insulator not shown have a high dielectric constant. The configuration of two power conductors separated by an insulator, provides distributed capacitance between the power conductors, lowering the AC impedance of the system. In an alternative embodiment, no insulator other than air is positioned between the power conductor surfaces, however, this decreases system performance. Further, in this alternative configuration it is critical that the conductor surfaces do not touch to create a short.

In the preferred embodiment, the mounting platform **100** includes a support leg **116***c*. In the embodiment shown in FIGS. **1** and **3**, the support legs **116***c* are conductive structure that extends from the platform conductive frame **140**. In the configuration shown in FIGS. **1** and **3**, the support leg **116***c*

is preferably coupled to ground. In the configuration shown in FIG. 4, the support leg 116c is a stand-off that provides mechanical support but is not necessarily electrically coupled to ground.

In the embodiment shown in FIG. 2, the input power leg 116a, the output power leg 116b, and the support leg 116c are electrically and mechanically coupled to the platform-printed circuit board 110. Various connection means may be used for connecting the input power leg 116a, output power leg 116b and support leg 116c including soldering the legs 116a–116c to the platform printed circuit board 110 or alternatively by using the bus bar described in the patent application entitled "A Power Bus Bar for Providing a Low Impedance Connection between a First and Second Printed Circuit Board" filed May 14, 1997 which is hereby incorporated by reference. However, in the preferred embodiment a second end of the output power leg 116b and a second end of the input power leg 116a are mechanically and electrically coupled to the platform PCB using a fastening means 174 and the first end of the output power leg 116b and the first end of the input power leg 116a are mechanically and electrically coupled to the base PCB 124 by soldering the first end of the output power leg 116b and the input power leg 116a to the base PCB 124.

Preferably the first end of the mounting platform legs 116a–c is narrowed to form one or more tabs for easy insertion into the base printed circuit board 124. The tab at the end of the platform legs is positioned adjacent to and in close proximity to the load (the microprocessor). Referring to FIG. 2, the tab at the end of the platform legs is typically soldered to the base printed circuit board which provides a good electrical and mechanical connection. The soldering can be of the "through-hole" type (illustrated) or the "surfacemount" type.

In the embodiment shown in FIG. 2, the first end of the first output conductor 144 and the first end of the second output conductor 150 are soldered to the base PCB 124. The first end of the first output conductor 144 is soldered to the first base electrical contact 136. The first end of the second output conductor 150 is soldered to the second base electrical contact (the ground plane). Similarly, the first end of the first input conductor and the first end of the second input conductor are soldered to the base PCB 124.

Because the first output conductor 144 is electrically coupled to a different electrical contact than the first input conductors 160, the voltage to which the first output conductor is preferably coupled is different than the voltage that the first input conductor is coupled to. For example, the first input conductor could be electrically coupled to a 5 volt input voltage while the first output conductor (the power going to the microprocessor) could be coupled to a 3.3 volt output voltage.

Referring to FIG. 2, the second end of the output conductor 144 is electrically coupled to the platform PCB 110 using a fastening means 174 which applies pressure to push the two output conductors together to make a good electrical contact to both surfaces of the platform PCB. The fastening means 174, typically includes a screw which is inserted through openings in the platform PCB, the first and second output conductors and a threaded fastener 176, 144, 150.

Typically, both the platform printed circuit board 110 and the base printed circuit board 124 have a power plane and a ground plane. Preferably, the first electrical contact 132 of the platform printed circuit board is connected to the power plane of the platform printed circuit board and the first electrical contact 136 of the base printed circuit board is electrically coupled to the power plane. Similarly, in the preferred embodiment the second electrical contact 134 of the platform printed circuit board is connected to the ground plane of the platform printed circuit board and the second electrical contact 138 of the base printed circuit board is electrically coupled to the ground plane of the base printed circuit board.

The first output conductor is electrically coupled to the first electrical contact of the platform PCB and the first electrical contact of the base PCB. Similarly, the second output conductor is electrically coupled to the second electrical contact of the platform PCB and the second electrical contact of the base PCB. Thus, the output power leg electrically connects the output voltage of the voltage regulator to the power plane of the base PCB and electrically connects the ground plane of the platform PCB to the ground plane of the base PCB. The first output conductor typically carries the output power of the voltage regulator to the microprocessor. The second output conductor connects the ground plane of the platform PCB to the ground plane of the base PCB.

Typically, the platform printed circuit board 110 has a third electrical contact formed on the first surface of the platform PCB 110 and a fourth electrical contact formed on the second surface of the platform PCB. Similarly, the base printed circuit board 124 has third electrical contact formed on the second surface of the base PCB 110 and a fourth electrical contact formed on the first surface of the base PCB. Preferably, the third electrical contact of the platform PCB is electrically coupled to the third electrical contact of the base printed circuit board by the first input conductor. Similarly, in the preferred embodiment the fourth electrical contact of the platform PCB is connected to the fourth electrical contact of the base PCB by the second input conductor.

The first input conductor is electrically coupled to the third electrical contact of the platform PCB and the third electrical contact of the base PCB. Similarly, the second input conductor is electrically coupled to the fourth electrical contact of the platform PCB and the fourth electrical contact of the base PCB. Thus, the input power leg electrically connects the input power plane of the platform PCB to the appropriate power plane of the base PCB and electrically connects the input ground plane of the platform PCB to the ground plane of the base PCB. The first input conductor typically carries the input power to the voltage regulator. The second input conductor connects the ground plane of the platform PCB to the ground plane of the base PCB.

The elongate legs 116a–c are positioned so that first surface of base printed circuit board is generally parallel to the first surface of the platform printed circuit board. In an alternative embodiment, the mounting platform includes only an output power leg 116b and not an input power leg. In this case, the input power must be electrically coupled to the device on the mounting platform in an alternative fashion. For example, the input power might be connected to the platform PCB using a cable that is electrically coupled to the base PCB.

FIG. 3 shows a partial exploded view of the mounting platform shown in FIG. 1. In the embodiment shown in FIG. 3, the platform top 108 is comprised of a platform printed circuit board 110 and a platform conductive frame 140. In the embodiment shown in FIG. 3, the second input conductor and the second output conductor extend from the platform conductive frame. Typically, the platform conductive frame is positioned underneath the second surface of the platform printed circuit board. Typically the platform con-

ductive frame is electrically coupled to the ground and is used as the ground plane for the voltage regulator circuit and for conducting ground current through the second output conductor and the second input conductors to the base PCB. Although preferably the platform conductive frame is a unitary structure, it may include openings to prevent shorting of conductive components on the second surface of the platform PCB.

FIG. 4 shows a mounting platform according to an alternative embodiment of the present invention. In the embodiment shown in FIG. 3, the platform top is comprised of a platform PCB and does not include a platform conductive frame as is shown in the embodiment in FIGS. 1–3. FIG. 5 shows a side cross-sectional view of the output leg of the mounting platform shown in FIG. 4. Comparing FIG. 3 to FIG. 5, the second output conductor **150** shown in FIG. 5 is a separate structure and is not formed as a unitary part of the ground plane of the platform PCB.

It is understood that the above description is intended to be illustrative and not restrictive. For example, the structure of the input power leg and the output power leg are similar and typically functional and structural statements made for the input power leg are analagous to the output power leg. The scope of the invention should therefore be determined not with reference to the above description, but instead should be determined with reference to the appended claims, along with the full scope of equivalents to which such claims are entitled.

What is claimed is:

1. A mounting platform configuration, comprising:

a platform top including a platform printed circuit board, the platform printed circuit board including a first electrical contact formed on a first surface of the platform printed circuit board and a second electrical contact formed on a second surface of the platform printed circuit board;

a first device mounted on the first surface of the platform printed circuit board, wherein the first device is electrically coupled to the platform printed circuit board;

a base printed circuit board, the base printed circuit board including a first electrical contact formed on a second surface of the base printed circuit board and a second electrical contact formed on a first surface of the base printed circuit board;

a second device mounted on the first surface of the base printed circuit board; and

a plurality of conductive legs, including at least one output leg for mechanically supporting the platform printed circuit board in a position above the base printed circuit board such that the second surface of the platform printed circuit board is positioned above the first surface of the base printed circuit board by a distance that is at least a thickness of the second device, the output leg including a first output conductor and a second output conductor, wherein the first output conductor is generally parallel to the second output conductor, wherein the first output conductor is electrically isolated from the second output conductor, wherein the first output conductor is electrically coupled to the first electrical contact of the platform printed circuit board and the first electrical contact of the base printed circuit board, wherein the second output conductor is electrically coupled to the second electrical contact of the platform printed circuit board and the second electrical contact of the base printed circuit board, wherein the output leg and the platform top are electrically and mechanically coupled by a fastening means.

2. The mounting platform configuration recited in claim 1 wherein the platform printed circuit board further includes a third electrical contact and a fourth electrical contact, wherein the base printed circuit board further includes a third electrical contact and a fourth electrical contact, wherein the plurality of conductive legs further includes at least one input leg, the input leg including a first input conductor and a second input conductor, wherein the first input conductor is generally parallel to the second input conductor, wherein the first input conductor is electrically isolated from the second input conductor, wherein the first input conductor is electrically coupled to the third electrical contact of the platform printed circuit board and the third electrical contact of the base printed circuit board, wherein the second input conductor is electrically coupled to the fourth electrical contact of the platform printed circuit board and the fourth electrical contact of the base printed circuit board.

3. The mounting platform configuration recited in claim 2 wherein the first device is a voltage regulator and the second device is a microprocessor.

4. The mounting platform configuration recited in claim 3 wherein the mounting platform is placed adjacent to, but not directly over the microprocessor.

5. The mounting platform recited in claim 3 wherein the output leg is a leg carrying power from the voltage regulator to the microprocessor, wherein the output leg is placed in close proximity to the microprocessor.

6. The mounting platform configuration recited in claim 2, further including an input leg insulator positioned between the first input conductor and the second input conductor.

7. The mounting platform configuration recited in claim 2 wherein the output conductor and the second output conductor form a low impedance transmission line at high frequencies.

8. The mounting platform configuration recited in claim 1, further including an output leg insulator positioned between the first output conductor and the second output conductor.

9. The mounting platform configuration recited in claim 8 wherein the output leg insulator has a high dielectric constant.

10. The mounting platform configuration recited in claim 1 wherein the platform printed circuit board includes a ground plane electrically coupled to the second electrical contact of the platform printed circuit board.

11. the mounting platform configuration recited in claim 1 further including a platform conductive frame wherein the second output conductor of the output leg extends from the platform conductive frame.

12. The mounting platform configuration recited in claim 1, wherein at least one support leg extends from the platform conductive frame to provide additional mechanical support.

13. The mounting platform configuration recited in claim 11, wherein the platform conductive frame is electrically coupled to a ground plane.

14. The mounting platform configuration recited in claim 11, wherein the fastening means is a screw.

15. A mounting platform configuration, comprising:

a platform top including a platform conductive frame and a platform printed circuit board, the platform printed circuit board including a first electrical contact formed on a first surface of the platform printed circuit board and a second electrical contact formed on a second surface of the platform printed circuit board;

a first device mounted on the first surface of the platform printed circuit board, wherein the first device is electrically coupled to the platform printed circuit board;

a base printed circuit board, the base printed circuit board including a first electrical contact formed on a second surface of the base printed circuit board and a second electrical contact formed on a first surface of the base printed circuit board;

a second device mounted on the first surface of the base printed circuit board; and

a plurality of conductive legs, including at least one input leg and at least one output leg for mechanically supporting the platform printed circuit board in a position above the base printed circuit board such that the second surface of the platform printed circuit board is positioned above the first surface of the base printed circuit board by a distance that is at least a thickness of the second device, the output leg including a first output conductor and a second output conductor, wherein the first output conductor is generally parallel to the second output conductor, wherein the first output conductor is electrically isolated from the second output conductor, wherein the first output conductor is electrically coupled to the first electrical contact of the platform printed circuit board and the first electrical contact of the base printed circuit board, wherein the second output conductor is electrically coupled to the second electrical contact of the platform printed circuit board and the second electrical contact of the base printed circuit board; wherein a first end of the input leg is electrically and mechanically coupled to the base printed circuit board by soldering.

* * * * *